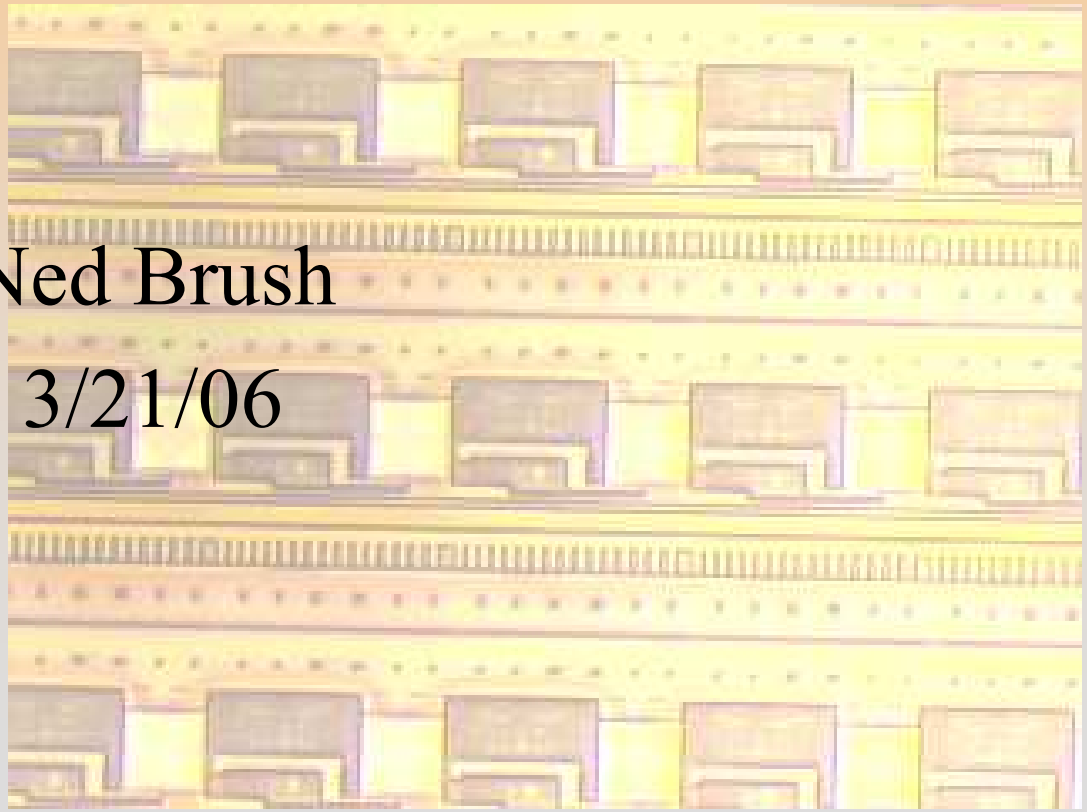
Chip Building Practicum



Ned Brush

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My Background

- Compaq Alpha
  - EV79
- Sonic Window
  - Mixed-signal
  - Fully custom

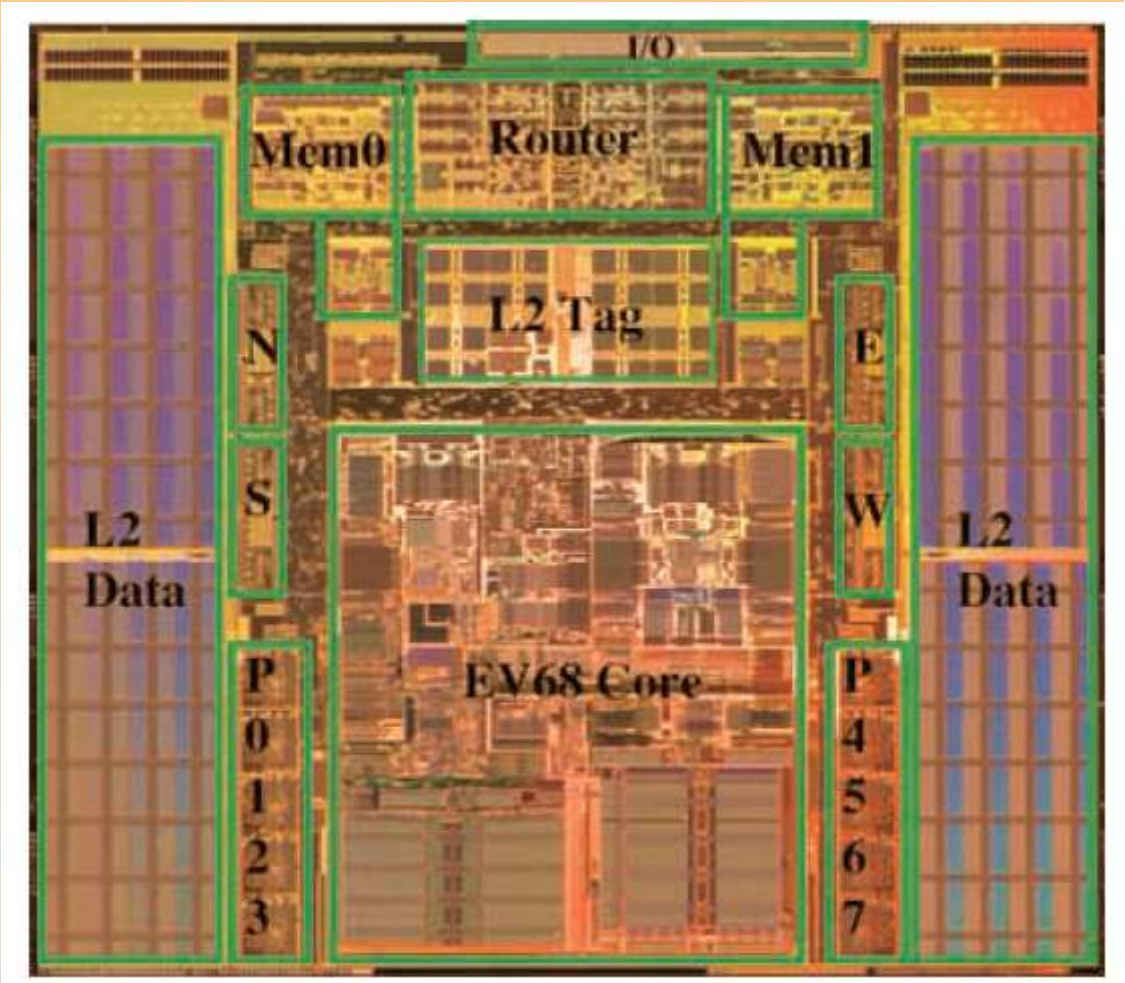
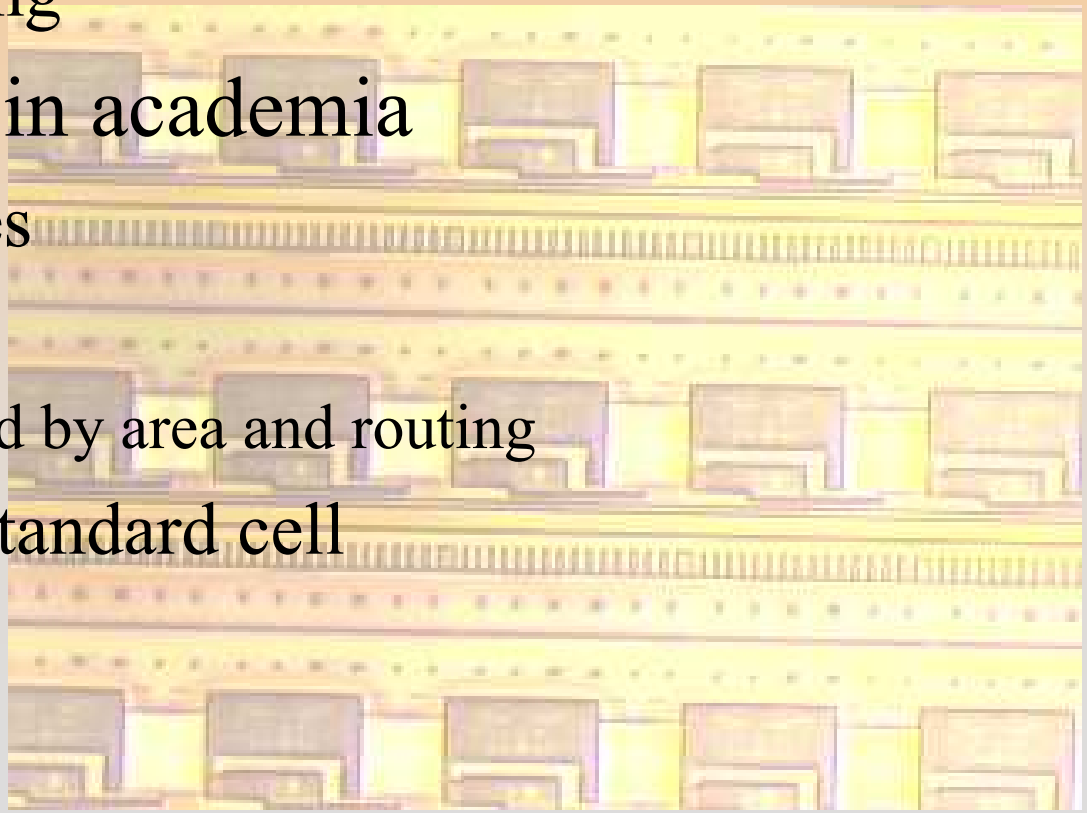


Figure reference: http://h18002.www1.hp.com/alphaserver/download/Compaq_EV7_Wp.pdf

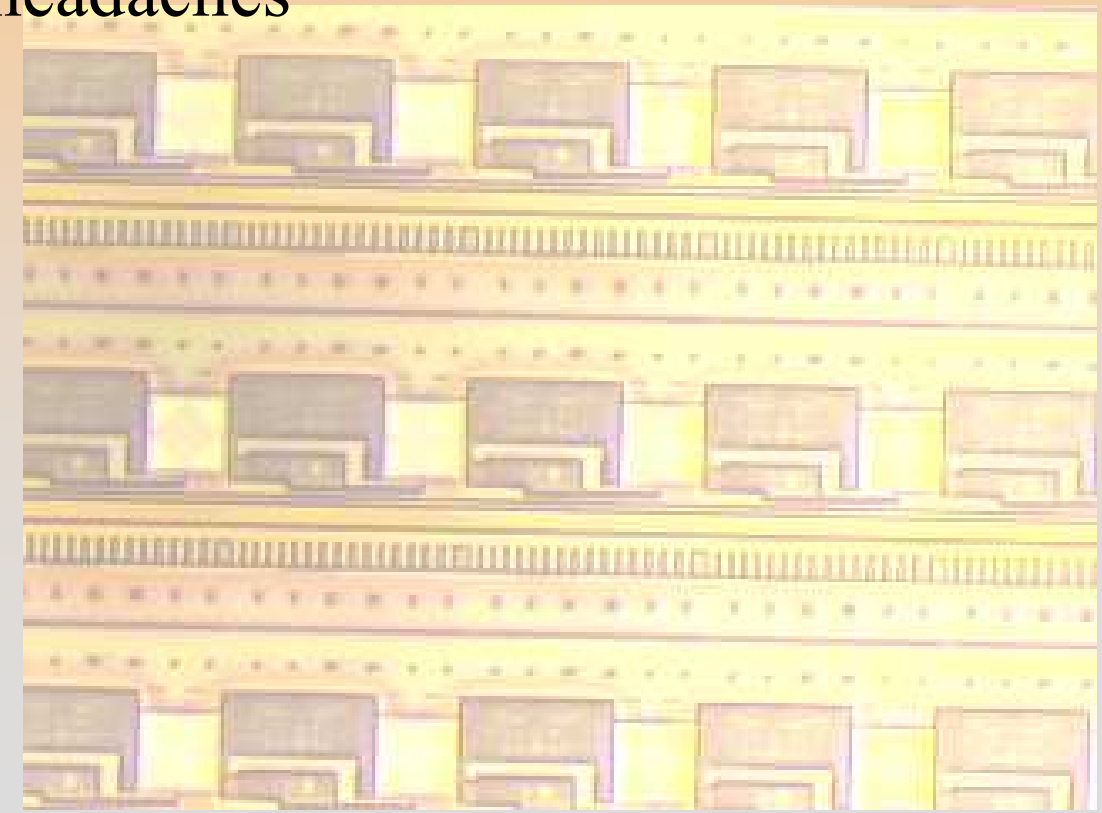
Application Specific Nature

- Designing CPU's
  - Large undertaking
- Designing chips in academia
  - Tighter deadlines
  - Test chips
    - Less constrained by area and routing
  - Full custom or standard cell



Multi-developer environment

- File naming
  - Leads to many headaches
- Versioning
  - TDM



Specifications

- First big step in procedure
- Formal specifications less feasible in academia (or R&D)
  - Functionality
  - Interface
  - Testability

External Interface

- Packaging
  - I/O limited
  - Area limited
- PCB considerations
  - Test PCB
  - Sonic Window PCB

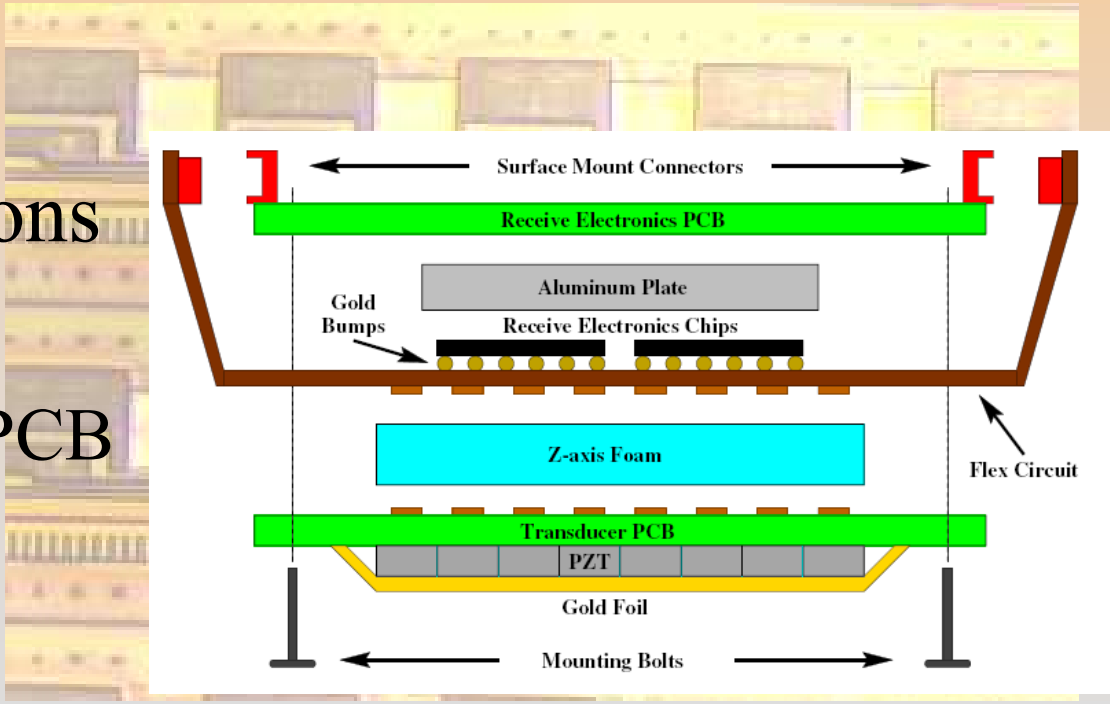
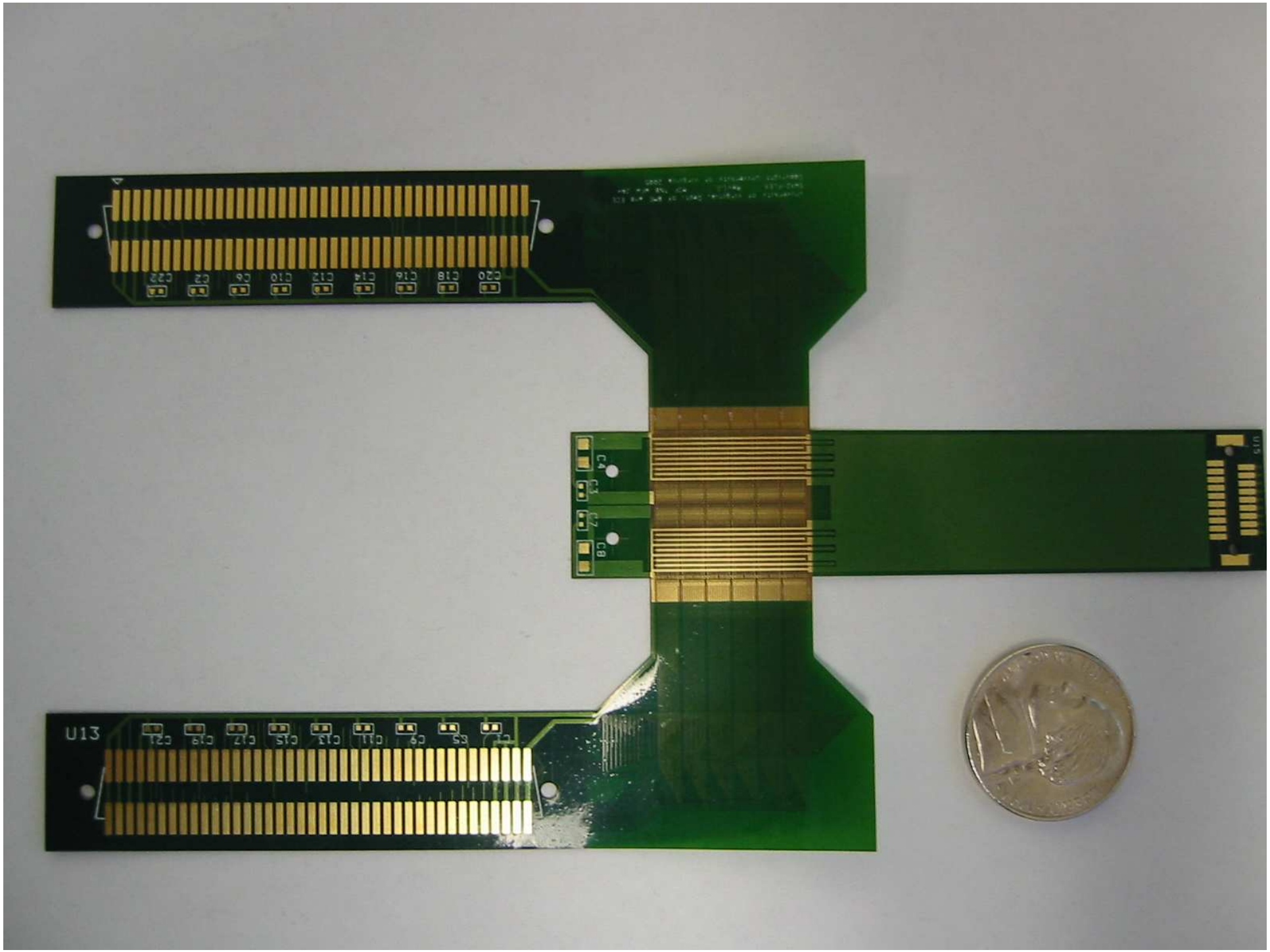


Figure reference: The Sonic Window: Second Generation Prototype of Low-Cost, Fully-Integrated, Pocket-Sized Medical Ultrasound Device; Michael Fuller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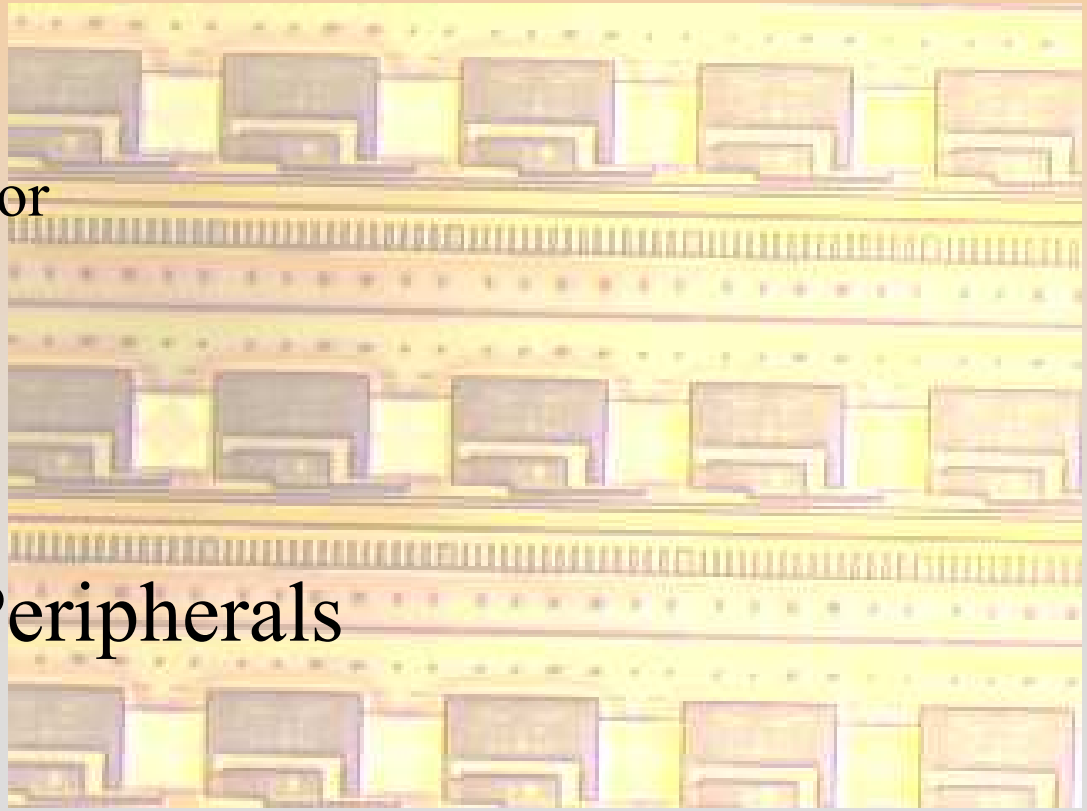
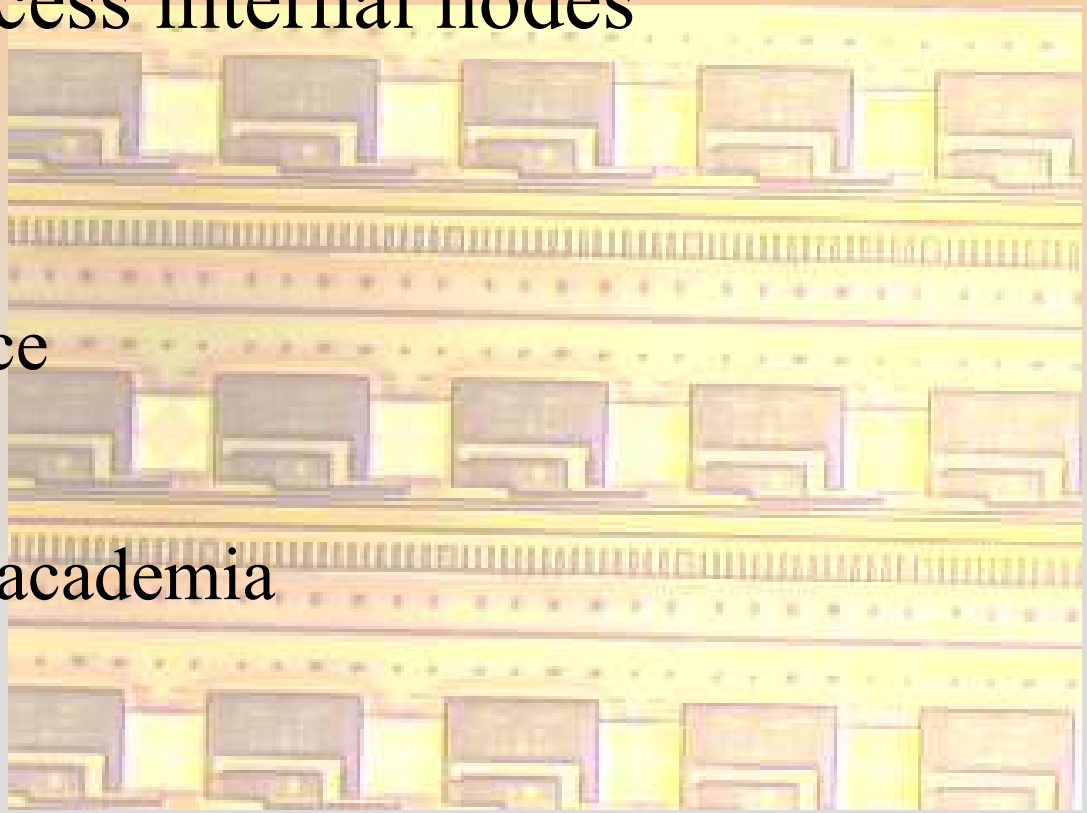
Off-chip concerns

- Components
  - Biasing
  - Digital Controls
    - Pattern Generator
    - FPGA
  - Test points
  - Regulators
- Sonic Window Peripherals



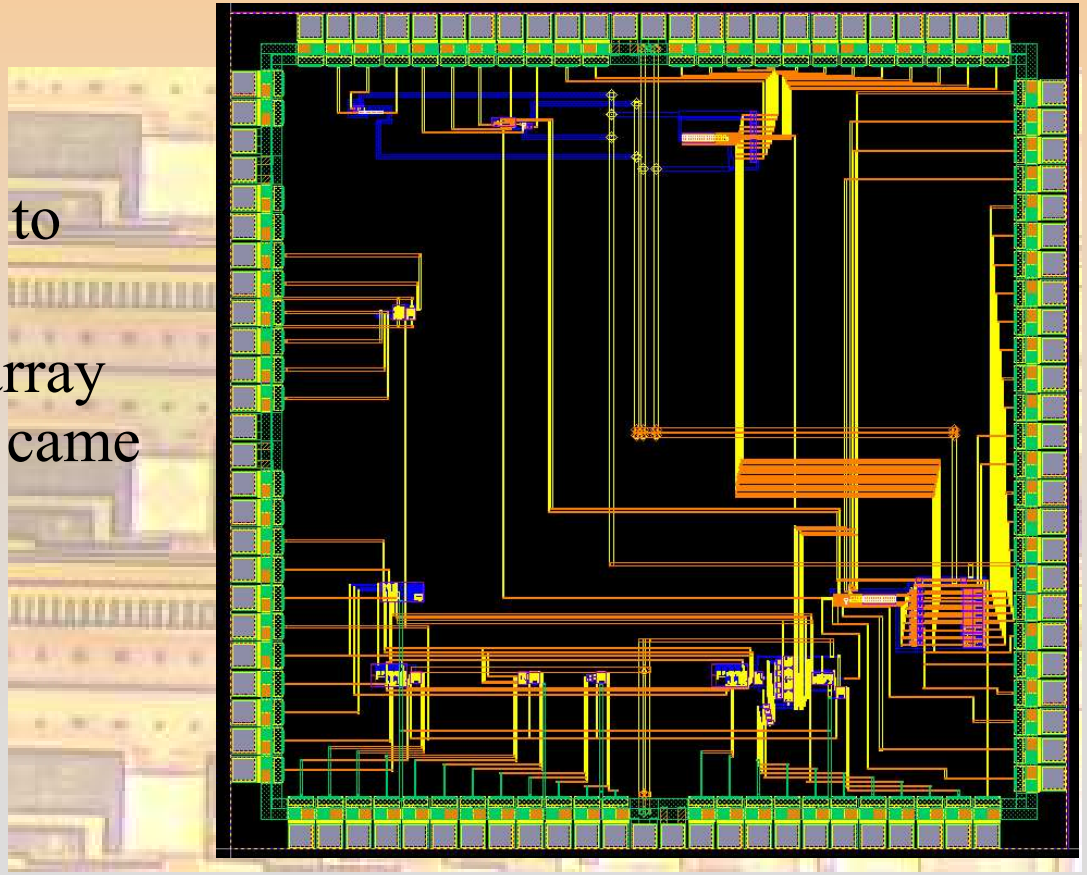
Testability

- Ability to fully characterize chip
- I/O buffers to access internal nodes
- Measurability
  - Equipment
  - External Interface
- BIST
  - Less feasible in academia



Testability cont'd

- Sonic Window example
  - Test chip
    - Wasn't feasible to test full array
    - Taped out full array before test chip came back
  - Test signals




File
Control
Setup
Measure
Analyze
Utilities
Help
4:14 AM
500 MSa/s
1.00 Mpts
1 On
2 On
3 On
4 On
200 mV/
On
Ax
Bx
d7 15
d6 14
d5 13
d4 12
d3 11
d2 10
d1 9
d0 8
f2
sel 4
cmpslp 3
san 6
pre 5
lsb 2
WE 1
4
More (1 of 2)
Delete All
H
10.0 µs/
1.0680570000 ms
0
T
1.168 V
Markers
Logic
Scales
X
Y
A——(f2) = 1.10660265 ms -44.6 mV
B---(4) = 1.03442455 ms 1.385 V
Δ = -72.17810 µs 1.4294 V
1/ΔX = -13.854619141 kHz

Tool Specific

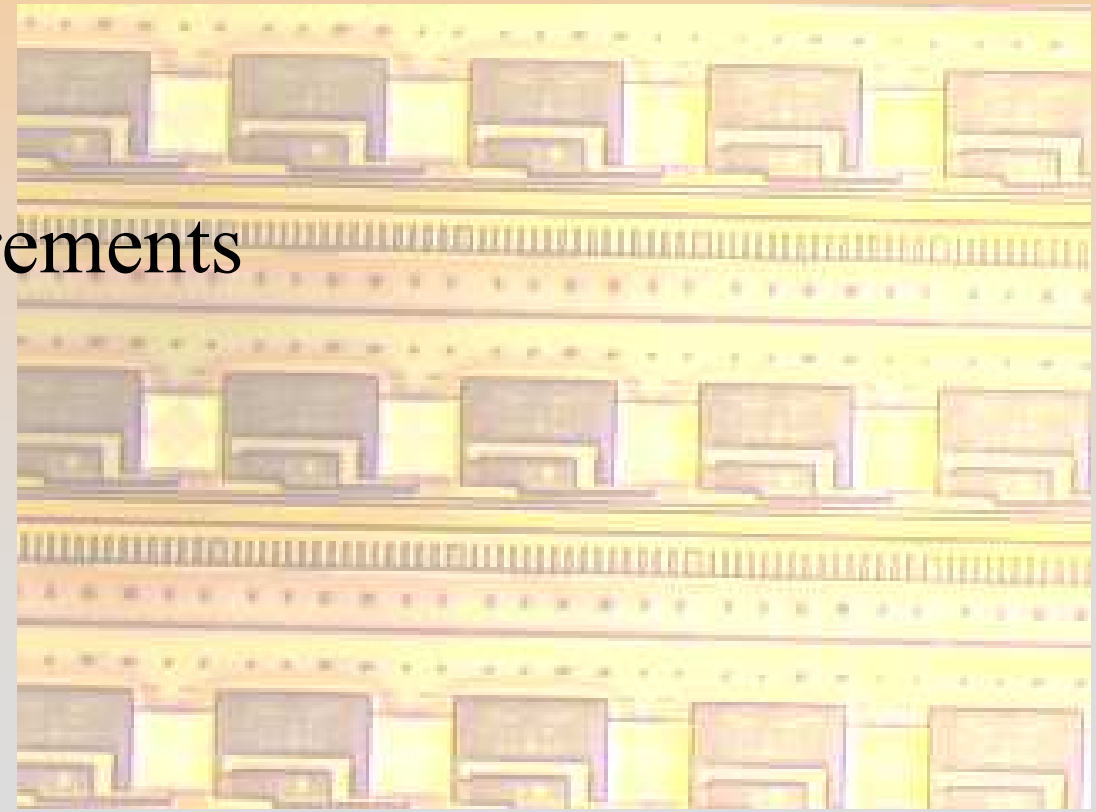
- Learning Cadence
  - Many tricks not found in many tutorials (i.e. F3 and mouse trails)
- DRC
- LVS
  - Hard-to-find errors (i.e. signals merged)
- SKILL
- OrCAD

Floorplanning

- Necessary if area is a concern
- Crosstalk concerns for mixed signal
- Matching analog transistors
- Sonic Window example
  - Analog priority

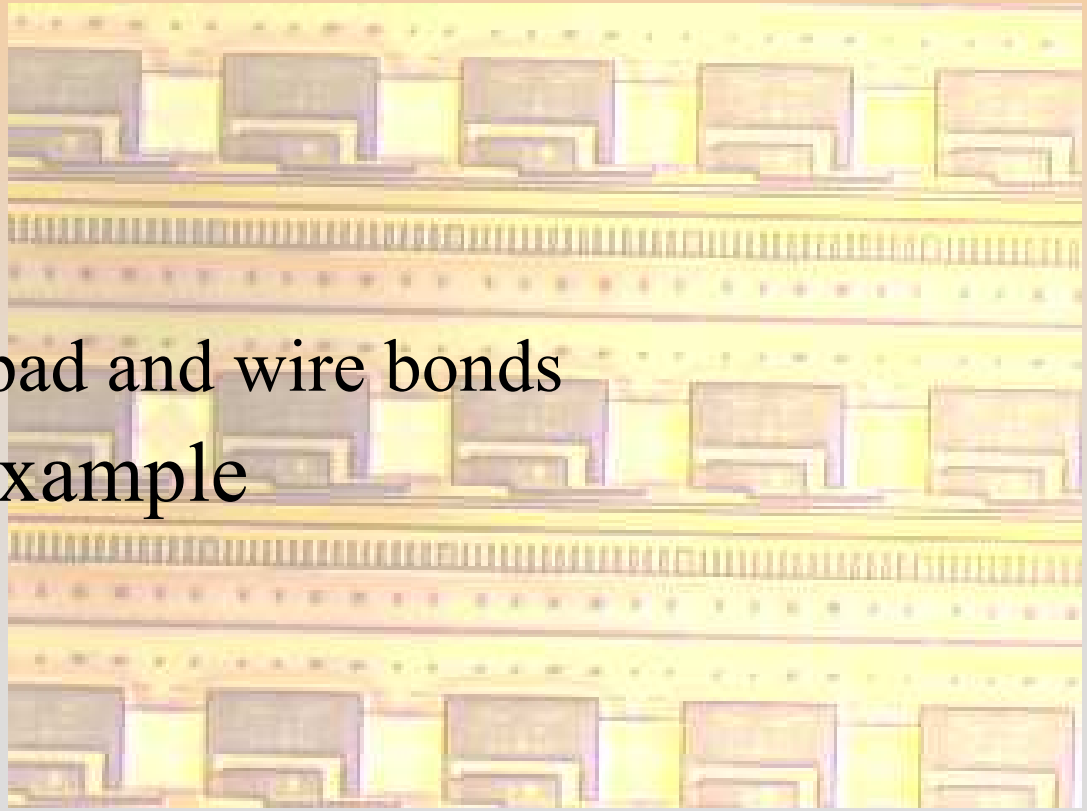
Technical

- Pad frame & ESD
- Power delivery
- Antenna Rules
- Metal Fill requirements
- Current Mirrors



Verification

- Mostly simulation based
  - Transient and AC
  - Corners
  - Parametrics
  - Extracted
  - Parasitics from pad and wire bonds
- Sonic Window example
  - AHDL



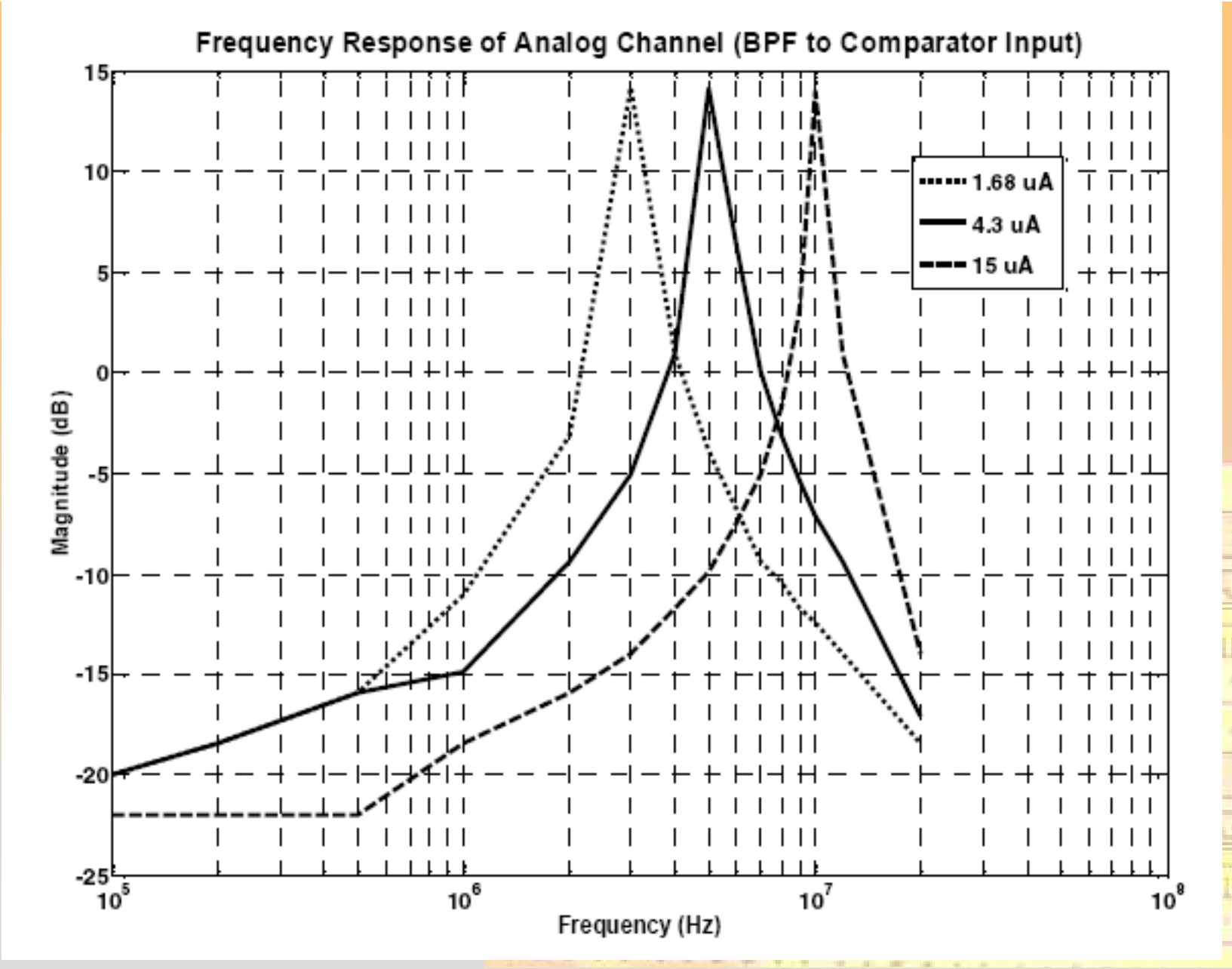
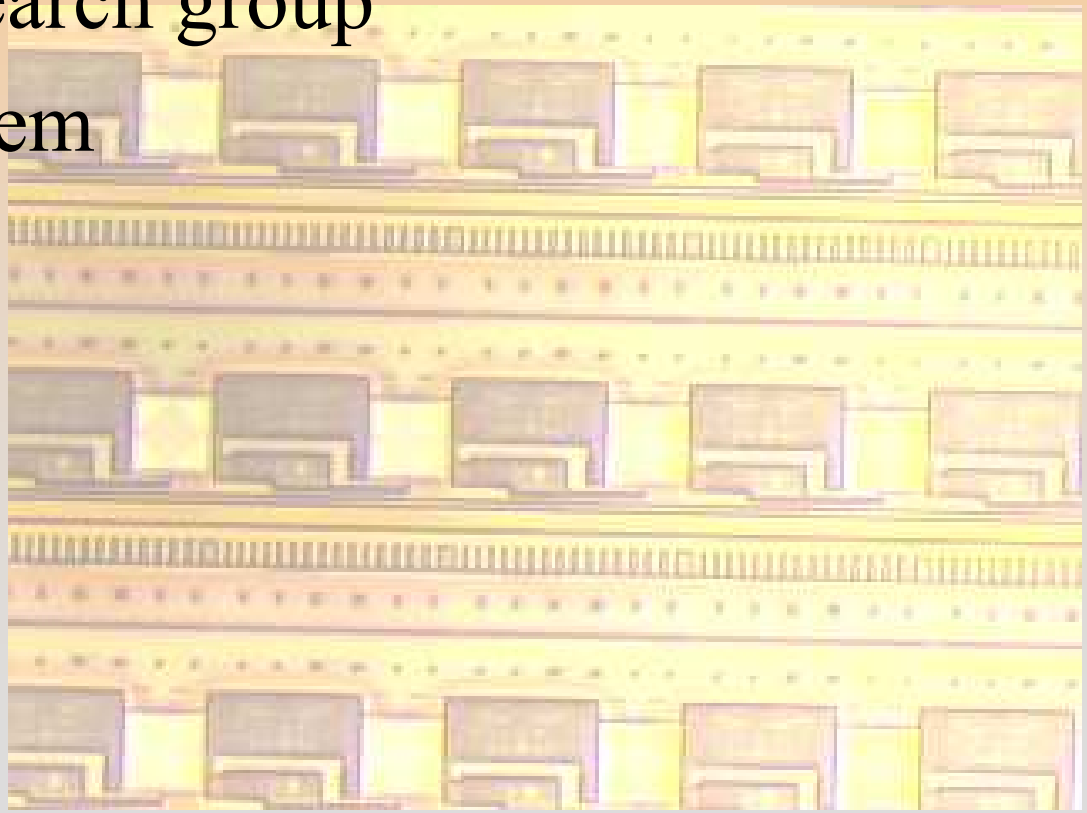


Figure reference: The Sonic Window: Second Generation Prototype of Low-Cost, Fully-Integrated, Pocket-Sized Medical Ultrasound Device; Michael Fuller

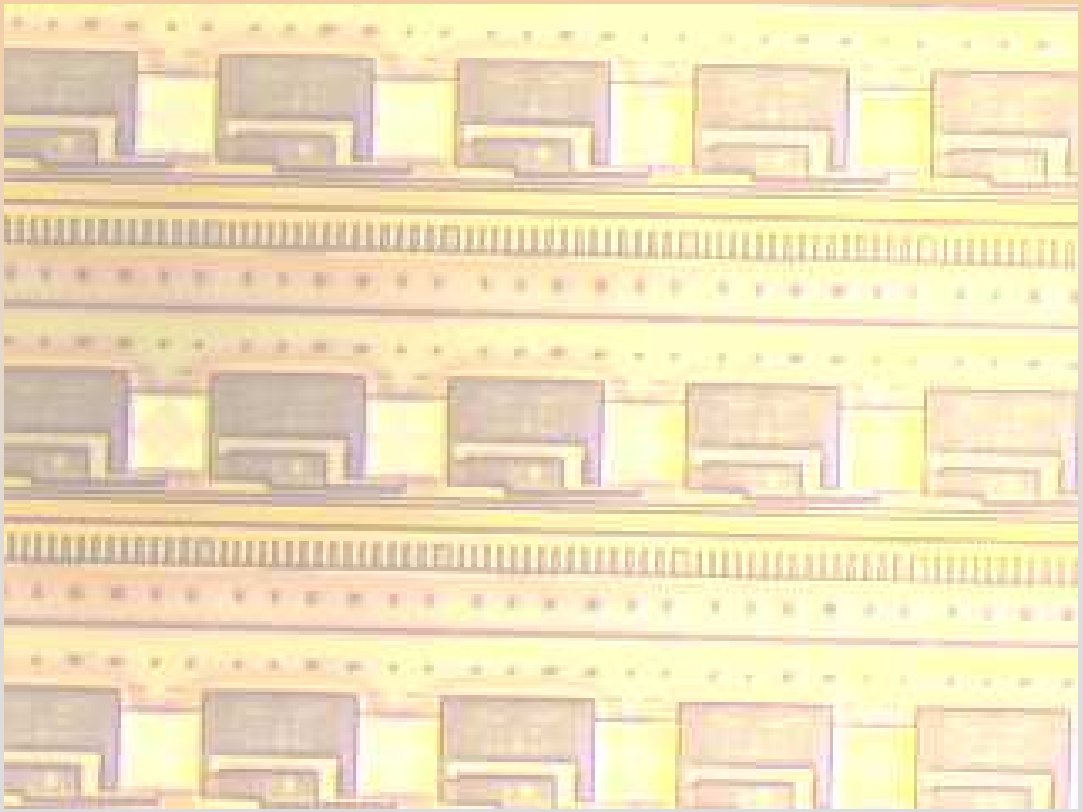
Design Reviews

- Schematic Freezing??
- Advisor and research group
- When to have them

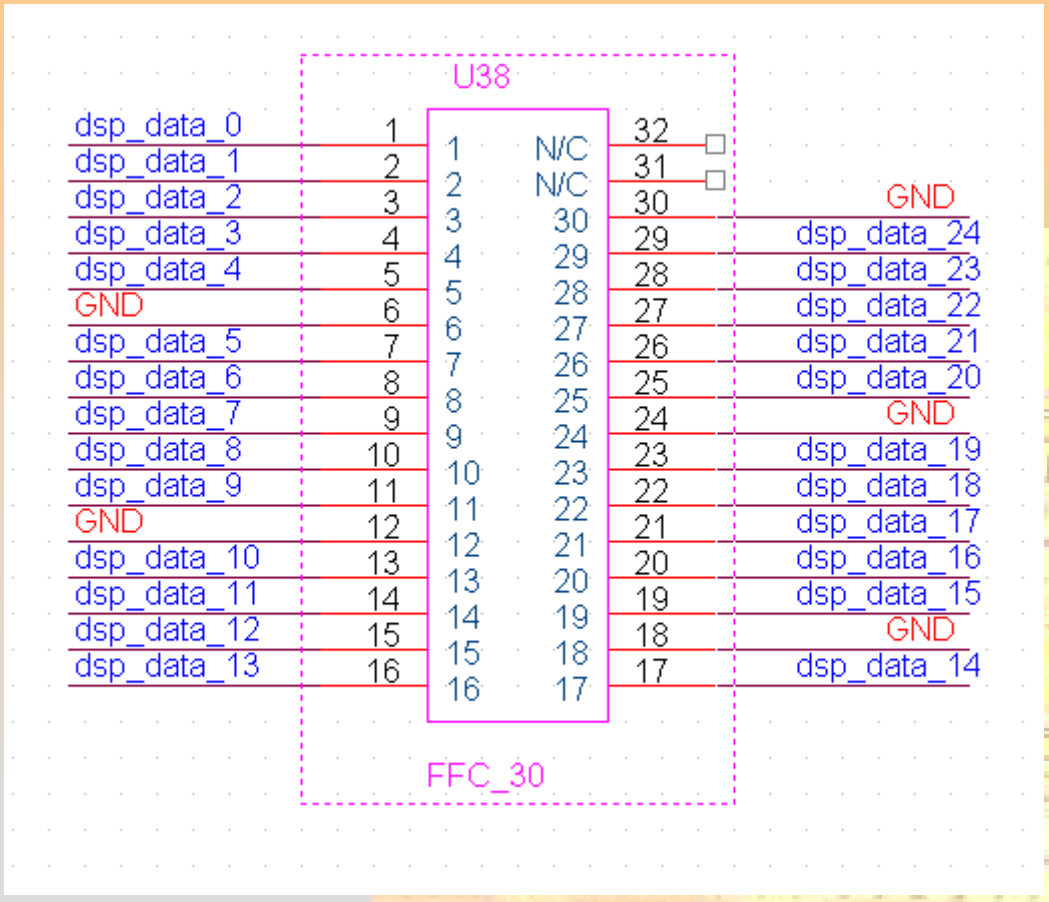


PCB Design

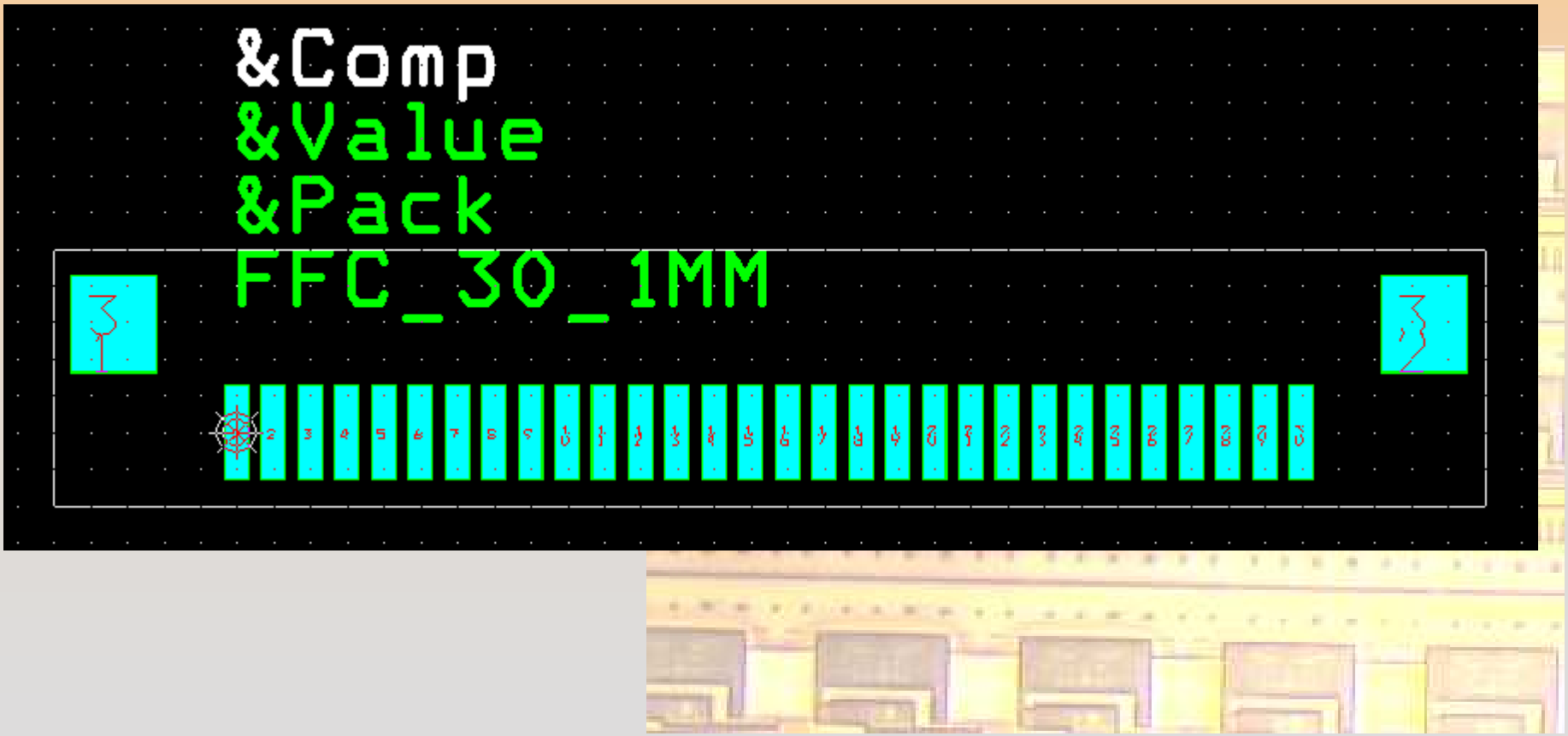
- OrCAD & Eagle



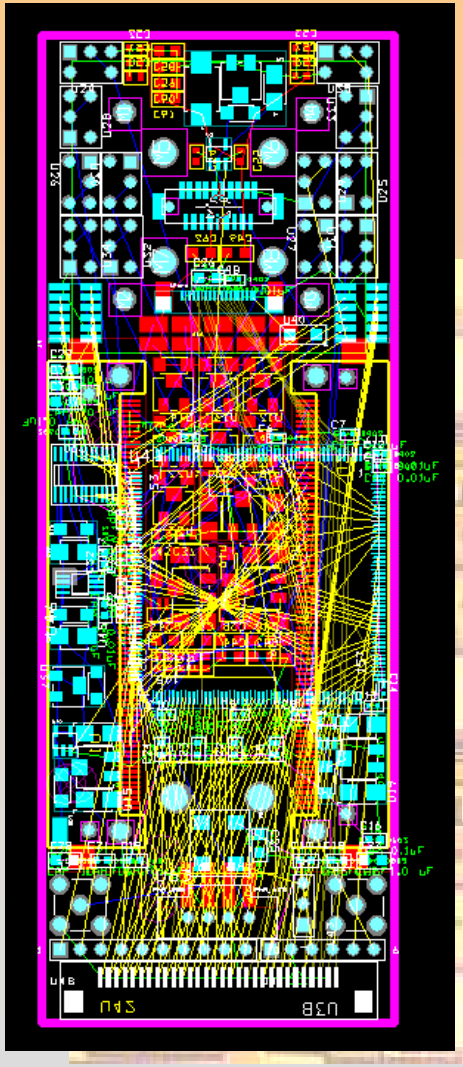
PCB Schematic



PCB Part

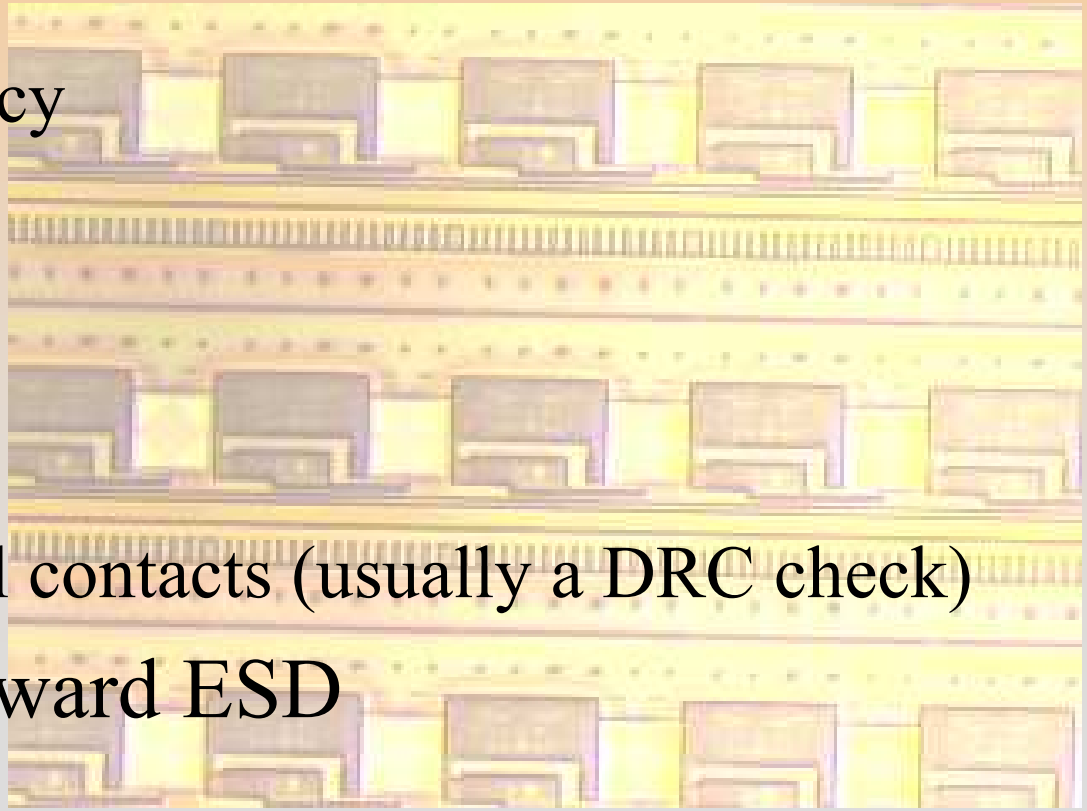


PCB Pre-routing



Common Mistakes

- High parasitics
  - Bad models
  - Limited frequency
- Crosstalk
- Mismatch
- Latch-up
  - Not enough well contacts (usually a DRC check)
- No ESD or backward ESD



Previous mistakes

- Forgot to hook up power/gnd
- Forgot to rename cell in hierarchy
- Current Mirror in Comparator
- Miscommunications & lack of formal specification
- Lack of good understanding of packaging technologies